Attorney's Docket No.: 07977-182002 / US341601

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Yamazaki, et al. Art Unit : 2823
Serial No.: 09/635,832 Examiner : Fernando Toledo
Filed : August 9, 2000
Title : SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR

Commissioner for Patents
Washington, D.C. 20231

RESPONSE

In response to the action mailed September 27, 2001, please amend the application as follows:

In the claims:

Please elect Group II, claims 18-37 and 39-40.

Please amend claim 18-20, 23, 25, and 28-37 as follows:

18. (Amended) An integrated circuit comprising:

a CMOS circuit; [having]

an n-channel field effect transistor and a p-channel field effect transistor in the CMOS circuit;

said n-channel field effect transistor comprising:

a crystalline semiconductor formed on an insulating surface;

a source region, a drain region and a channel forming region in the crystalline semiconductor;

a gate insulating film;

03/05/2002 SSITHIB1 00000044 09635832

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CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

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